module Control(

input [3:0]opcod,

output RegDest,

output ALUSrc,

output MemToReg,

output RegWrite,

output MemWrite,

output Branch,

output ALUop2,

output ALUop1,

output ALUop0,

output Jump

);

wire temp1;

wire temp2;

wire temp3;

wire temp4;

not N1(RegDest, opcod[3]);

and A1(ALUSrc, opcod[3], ~opcod[2]);

not N2(MemToReg, ~opcod[3]);

or OR(RegWrite, ~opcod[3], ~opcod[1]);

and A2(temp1, opcod[3], ~opcod[2]);

and A3(MemWrite, temp1, opcod[1]);

and A4(Branch, opcod[3], opcod[2]);

and A5(ALUop2, ~opcod[3], ~opcod[1]);

and A6(temp2, opcod[1], ~opcod[0]);

and A7(temp3, ~opcod[1], opcod[0]);

or O1(temp4, temp2, temp3);

or O2(ALUop1, opcod[3], temp4);

not N4(ALUop0, ~opcod[2]);

and A8(Jump, opcod[3], opcod[0]);

endmodule